## EEL 3701 – Digital Logic and Computer Systems Lab 1

## Greg Bolling

## UF ID 64911960

### Problem Statement

The goal of the lab was to build a first design for an FPGA circuit using an FPGA Out of The Box (OOTB) board, Intel Quartus and a new breakout board that I assembled. The breakout board is a new design board that has switches, LEDs, push buttons and a buzzer. There are wires used to connect the breakout board to the FPGA OOTB board.

In addition, the design was to implement two circuits, both simple circuits. Each was an input to output logic circuit that was hooked up to LED’s to see the output(s). The design was captured using VHDL (VHSIC Hardware Description Language) and run through a synthesis and then place and route process using Quartus and Modelsim simulator. Finally, before programming the board, he pins were assigned to locations so the circuit would know which wires to take as inputs and outputs.

### Design

The design consists of two basic circuits. The first circuit had inputs of .

The second circuit had six switch inputs and a single pushbutton input of SW1, SW2, SW3, SW4, SW5, SW6 and PB6 and it was for three LED outputs and a buzzer output (LED1, LED2, LED3 and BUZ.) The equations are all active true = high and are as follows:

LED1\_H = SW1\_H OR SW2\_H;

LED2\_H = NOT(SW3\_H XNOR SW4\_H);

LED3\_H = (NOT(SW5\_H) AND SW6\_H) OR PB6\_H;

BUZ\_H = (NOT(SW5\_H) AND SW6\_H) OR PB6\_H;

### Implementation

The circuit was implemented using the Quartus design tool to compile VHDL code form the same logic equations. The compiler synthesized the code and then it was placed and routed with pin assigned based on how I connected the FPGA board to the expansion board. I connected up the LED’s to the output pins of the LEDs from the FPGA board. I then connected the input pins from the expansion board to the inputs of the FPGA including the pushbutton switch. Finally, I connected the buzzer to the FPGA board. The pin numbers were important as they have to match the connected pins in the Quartus design tool.

The VHDL code had an entity and an architecture. The entity was like the pin out and the architecture is the implementation. The implementation of the logic design in VHDL where signals are all default to active high and was simple and looked like:

architecture Lab01\_arch of Lab01 is

begin

LED1 <= SW1 or SW2;

LED2 <= not(SW3 xnor SW4);

LED3 <= (not(SW5) and SW6) or PB6;

BUZ <= (not(SW5) and SW6) or PB6;

end Lab01\_arch;

### Testing

To test the FPGA board, I connected up the LED’s to the output pins of the LEDs from the FPGA board. I then connected the input pins from the expansion board to the inputs of the FPGA including the pushbutton switch. Finally, I connected the buzzer to the FPGA board.

To test the circuit, I switched the switches on and off to match the truth/voltage tables below in the Appendix. After verifying they all matched, I will show this to my peer instructor at the start of class.

### Conclusions

From this lab I assembled more circuits by soldering and became better at soldering. I also learned how to use Quartus to build a simple circuit and downloaded that circuit to the FPGA. I also learned that the jumper pin J5 on the FPGA board was important and has to be installed to program the FPGA using the JTAG header connector (it was missing and caused Quartus to not find the FPGA.) I learned basic VHDL code structure and how to connect signals to pin numbers in Quartus using FPGA Pin Assignment.

Appendix

Truth and Voltage Tables

The table of logic and voltage tables are:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Truth Table | | | Voltage Table | | |
| SW1 | SW2 | LED1 | SW1 | SW2 | LED1 |
| F | F | F | 0v | 0v | 0v |
| F | T | T | 0v | 5v | 5v |
| T | F | T | 5v | 0v | 5v |
| T | T | T | 5v | 5v | 5v |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Truth Table | | | Voltage Table | | |
| SW3 | SW4 | LED2 | SW3 | SW4 | LED2 |
| F | F | F | 0v | 0v | 0v |
| F | T | T | 0v | 5v | 5v |
| T | F | T | 5v | 0v | 5v |
| T | T | F | 5v | 5v | 0v |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Truth Table | | |  | Voltage Table | | |  |
| SW5 | SW6 | PB6 | LED3 / BUZ | SW5 | SW6 | PB6 | LED3 / BUZ |
| F | F | F | F | 0v | 0v | 0v | 0v |
| F | F | T | T | 0v | 0v | 5v | 5v |
| F | T | F | T | 0v | 5v | 0v | 5v |
| F | T | T | T | 0v | 5v | 5v | 5v |
| T | F | F | F | 5v | 0v | 0v | 0v |
| T | F | T | T | 5v | 0v | 5v | 5v |
| T | T | F | F | 5v | 5v | 0v | 0v |
| T | T | T | T | 5v | 5v | 5v | 5v |

Picture(s)